FEMTOCLOCKS™ CRYSTAL-TO-LVDS CLOCK GENERATOR

ICS844071

General Description

The ICS844071 is a Serial ATA (SATA)/Serial Attached SCSI (SAS) Clock Generator and a member of the HiPerClocks™ family of high performance devices from IDT. The ICS844071 uses an 18pF parallel resonant crystal over the range of 20.833MHz - 28.3MHz. For SATA/SAS applications, a 25MHz crystal is used and either 75MHz or 150MHz may be selected with the FREQ_SEL pin. The ICS844071 has excellent <1ps phase jitter performance, over the 900kHz - 7.5MHz integration range. The ICS844071 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

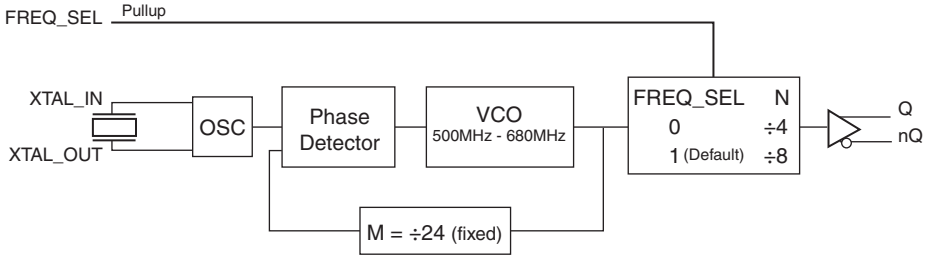
Features

- One differential LVDS output
- Crystal oscillator interface, 18pF parallel resonant crystal (20.833MHz – 28.3MHz)
- Output frequency range: 62.5MHz – 170MHz
- VCO range: 500MHz – 680MHz
- RMS phase jitter at 150MHz, using a 25MHz crystal (900kHz – 7.5MHz): 0.45ps (typical)
- Full 3.3V or 2.5V operating supply
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

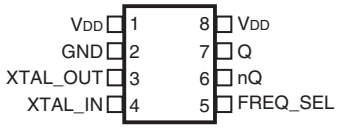
Table 1. Common Configuration Table

Inputs					Output Frequency (MHz)
Crystal Frequency (MHz)	FREQ_SEL	M	N	Multiplication Value M/N	
25	0	24	4	6	150
25	1	24	8	3	75
26.041666	0	24	4	6	156.25
26.041666	1	24	8	3	78.125
26.5625	0	24	4	6	159.375
26.5625	1	24	8	3	79.675

Block Diagram



Pin Assignment



ICS844071
8 Lead TSSOP
4.40mm x 3.0mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	$V_{DD}A$	Power		Analog supply pin.
2	GND	Power		Power supply ground.
3, 4	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	FREQ_SEL	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential output pair. LVDS interface levels.
8	V_{DD}	Power		Core supply pin.

NOTE: *Pullup* refers to intenal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characterisitcs* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	101.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 10%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.97	3.3	3.63	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.12	3.3	3.63	V
I_{DD}	Power Supply Current				135	mA
I_{DDA}	Power Supply Current				12	mA

Table 3B. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.12	2.5	2.625	V
I_{DD}	Power Supply Current				120	mA
I_{DDA}	Power Supply Current				12	mA

Table 3C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 10% or 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	V_{DD} = 3.3V	2		V_{DD} + 0.3	V
		V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	V_{DD} = 3.3V	-0.3		0.8	V
		V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.63V or 2.625V			5	µA
I_{IL}	Input Low Current	V_{DD} = 3.63V or 2.625V, V_{IN} = 0V	-150			µA

Table 3D. LVDS DC Characteristics, V_{DD} = 3.3V ± 10%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		275	365	455	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125	1.3	1.55	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 3E. LVDS DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		205	335	465	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		0.89	1.2	1.48	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		20.833		28.3	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

AC Electrical Characteristics

Table 5A. AC Characteristics, V_{DD} = 3.3V ± 10%, T_A = 0°C to 70°

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		62.5		170	MHz
$t_{jit}(\Phi)$	RMS Phase Jitter, Random; NOTE 1	150MHz, Integration Range: 900kHz – 7.5MHz		0.45		ps
		75MHz, Integration Range: 900kHz – 7.5MHz		0.46		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	150		400	ps
odc	Output Duty Cycle		48		52	%

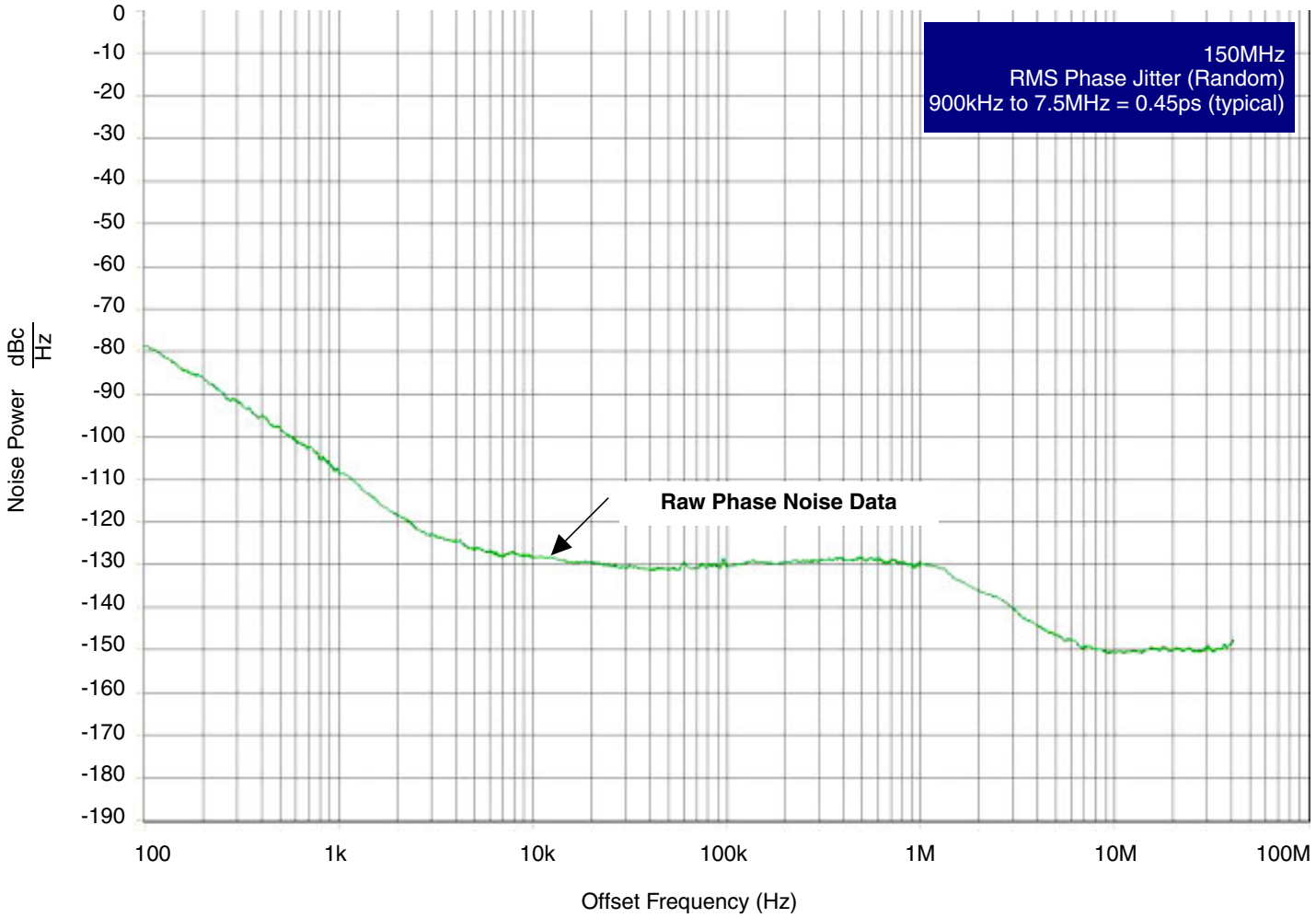
NOTE 1: Please refer to Phase Noise Plots.

Table 5B. AC Characteristics, V_{DD} = 2.5V ± 5%, T_A = 0°C to 70°

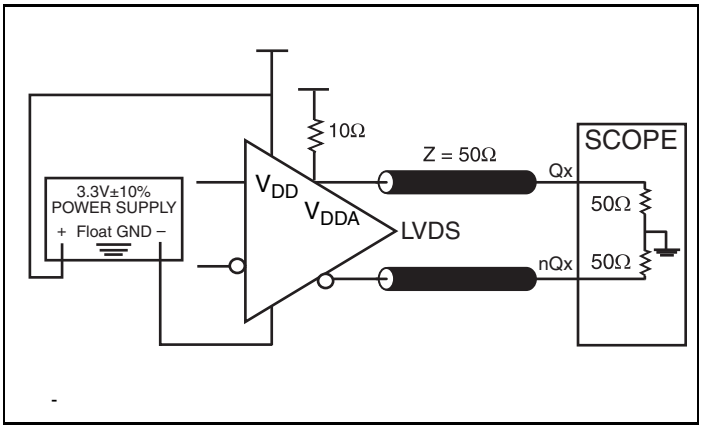
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		62.5		170	MHz
$t_{jit}(\Phi)$	RMS Phase Jitter, Random; NOTE 1	150MHz, Integration Range: 900kHz – 7.5MHz		0.56		ps
		75MHz, Integration Range: 900kHz – 7.5MHz		0.60		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	150		400	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Please refer to Phase Noise Plots.

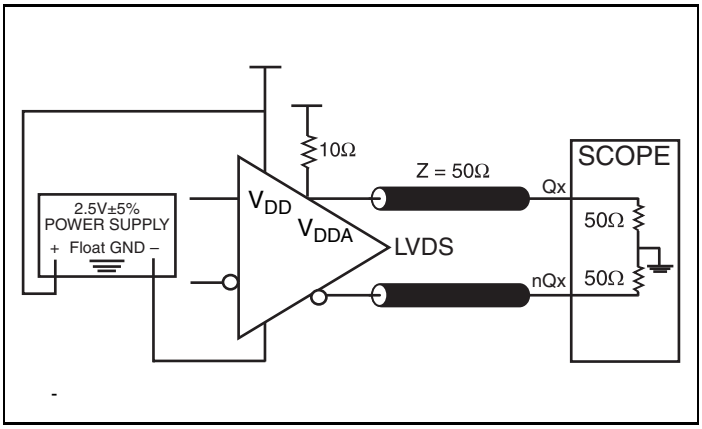
Typical Phase Noise at 150MHz (3.3V)



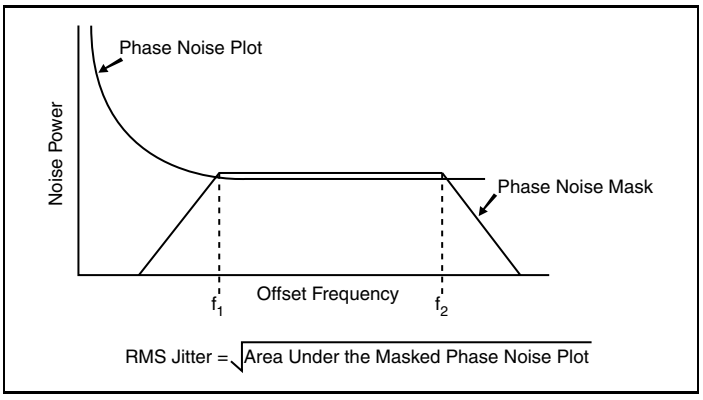
Parameter Measurement Information



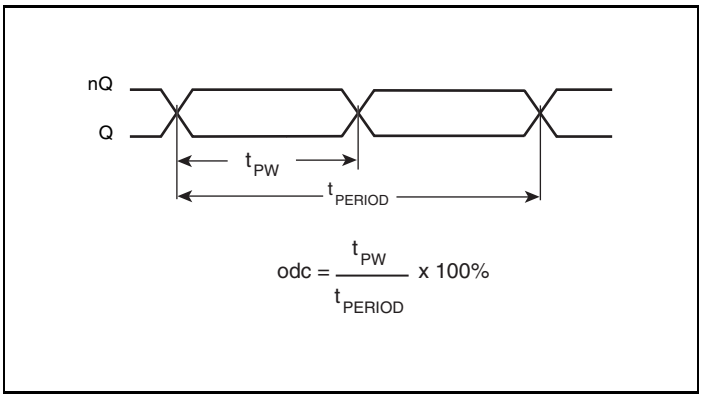
3.3V LVDS Output Load AC Test Circuit



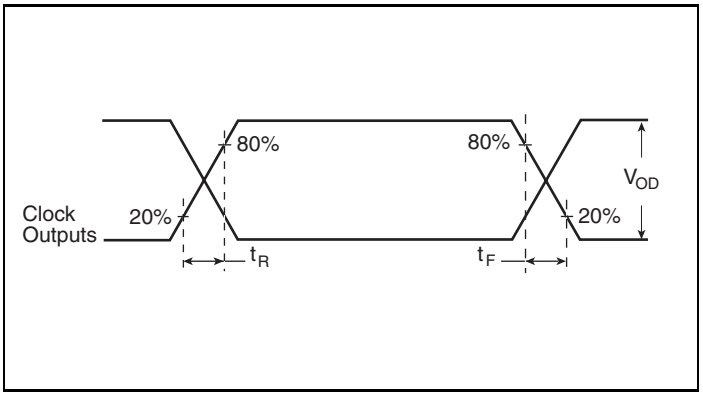
2.5V LVDS Output Load AC Test Circuit



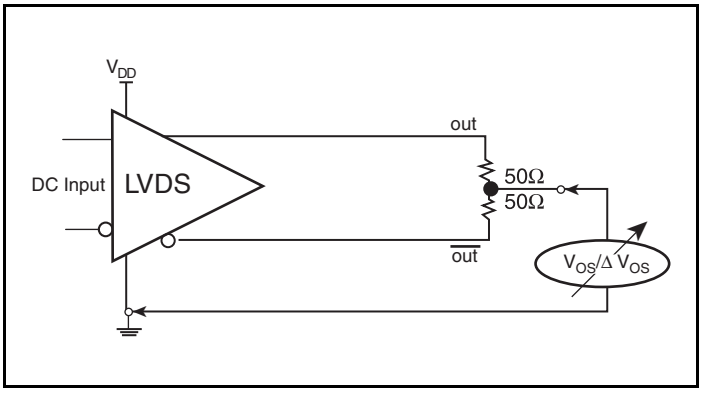
RMS Phase Jitter



Output Duty Cycle/Pulse Width/Period

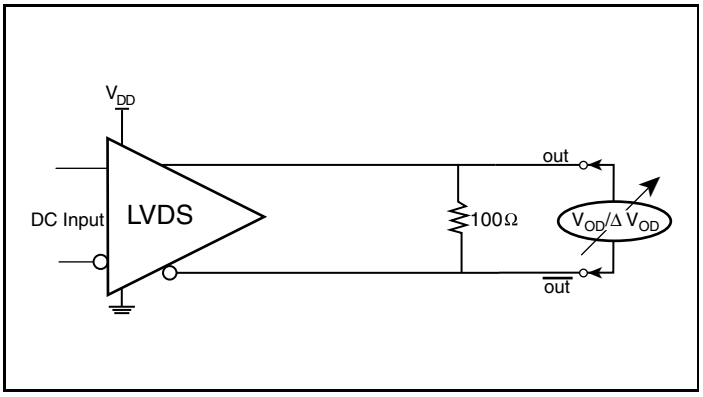


Output Rise/Fall Time



Offset Voltage Setup

Parameter Measurement Information, continued



Differential Output Voltage Setup

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS44071 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10μF and a 0.01μF bypass capacitor should be connected to each V_{DDA} pin.

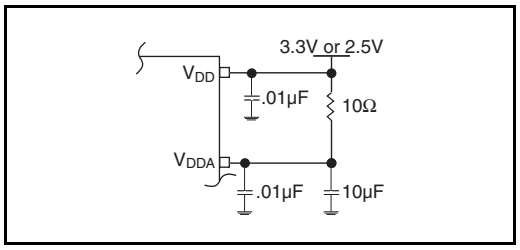


Figure 1. Power Supply Filtering

Crystal Input Interface

The ICS844071 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

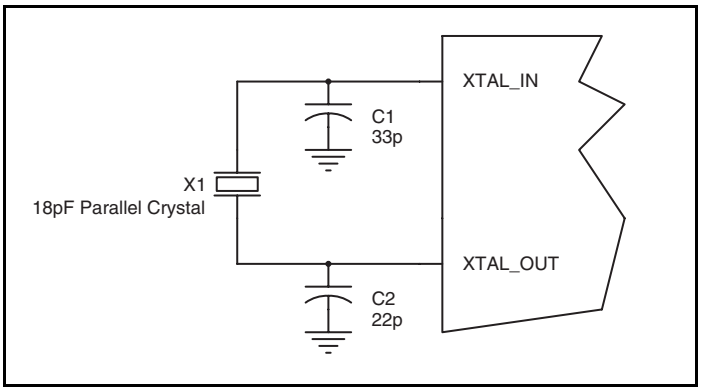


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

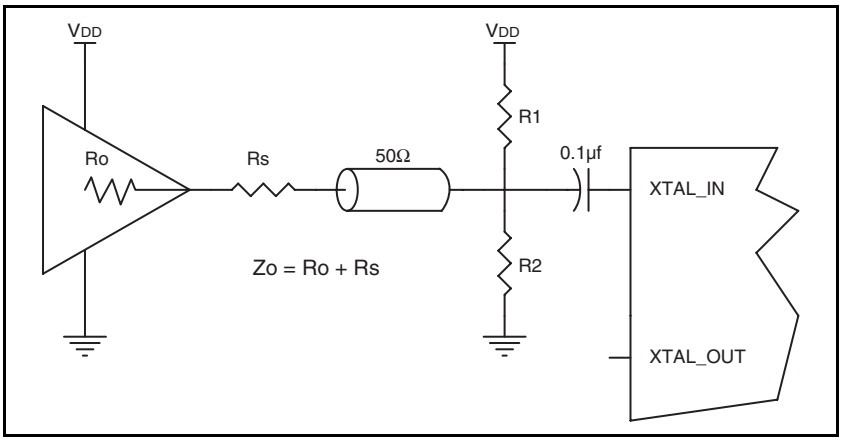


Figure 3. General Disgram for LVCMOS Driver to XTAL Input Interface

3.3V, 2.5V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input.

For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

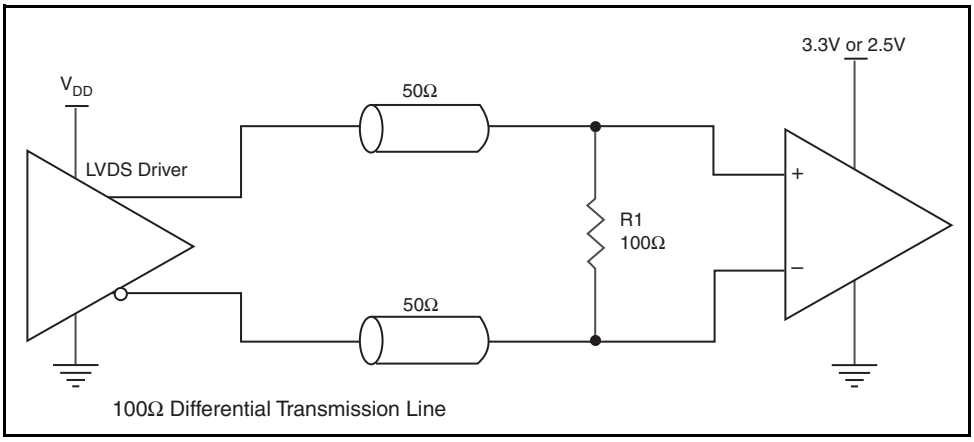


Figure 4. Tyical LVDS Driver Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844071.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844071 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 10% = 3.63V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.63V * (135mA + 12mA) = **533.61mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 90.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.533W * 90.5°C/W = 118.3°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 8 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5	89.8

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 8 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5	89.8

Transistor Count

The transistor count for ICS844071 is: 2533

Package Outline and Package Dimension

Package Outline - G Suffix for 8 Lead TSSOP

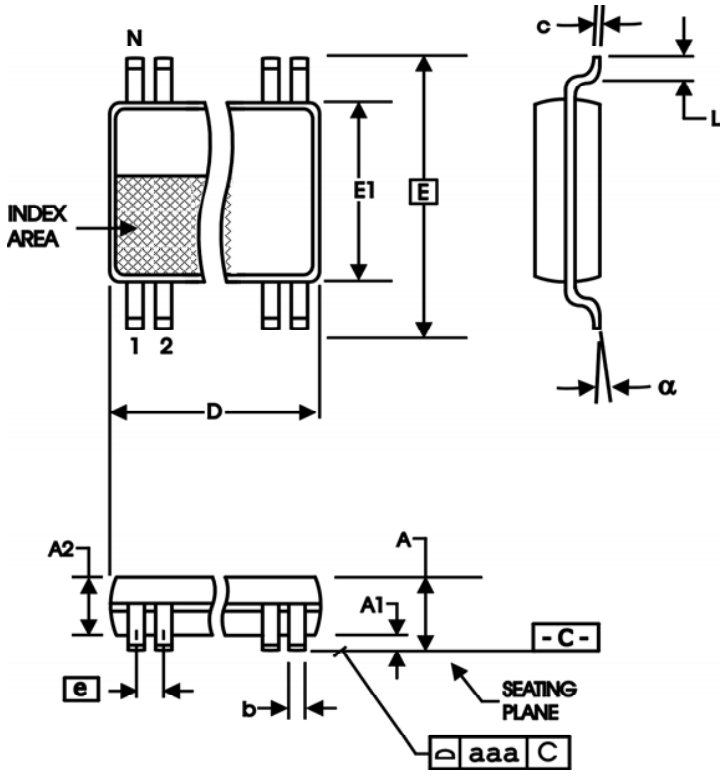


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS844071AG	4071A	8 Lead TSSOP	Tube	0°C to 70°C
ICS844071AGT	4071A	8 Lead TSSOP	2500 Tape & Reel	0°C to 70°C
ICS844071AGLF	071AL	“Lead-Free” 8 Lead TSSOP	Tube	0°C to 70°C
ICS844071AGLFT	071AL	“Lead-Free” 8 Lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T8	9 13	Added *LVCMOS to XTAL Interface* section. Ordering Information Table - added lead-free marking. Updated datasheet format.	9/26/07

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